PCB Power

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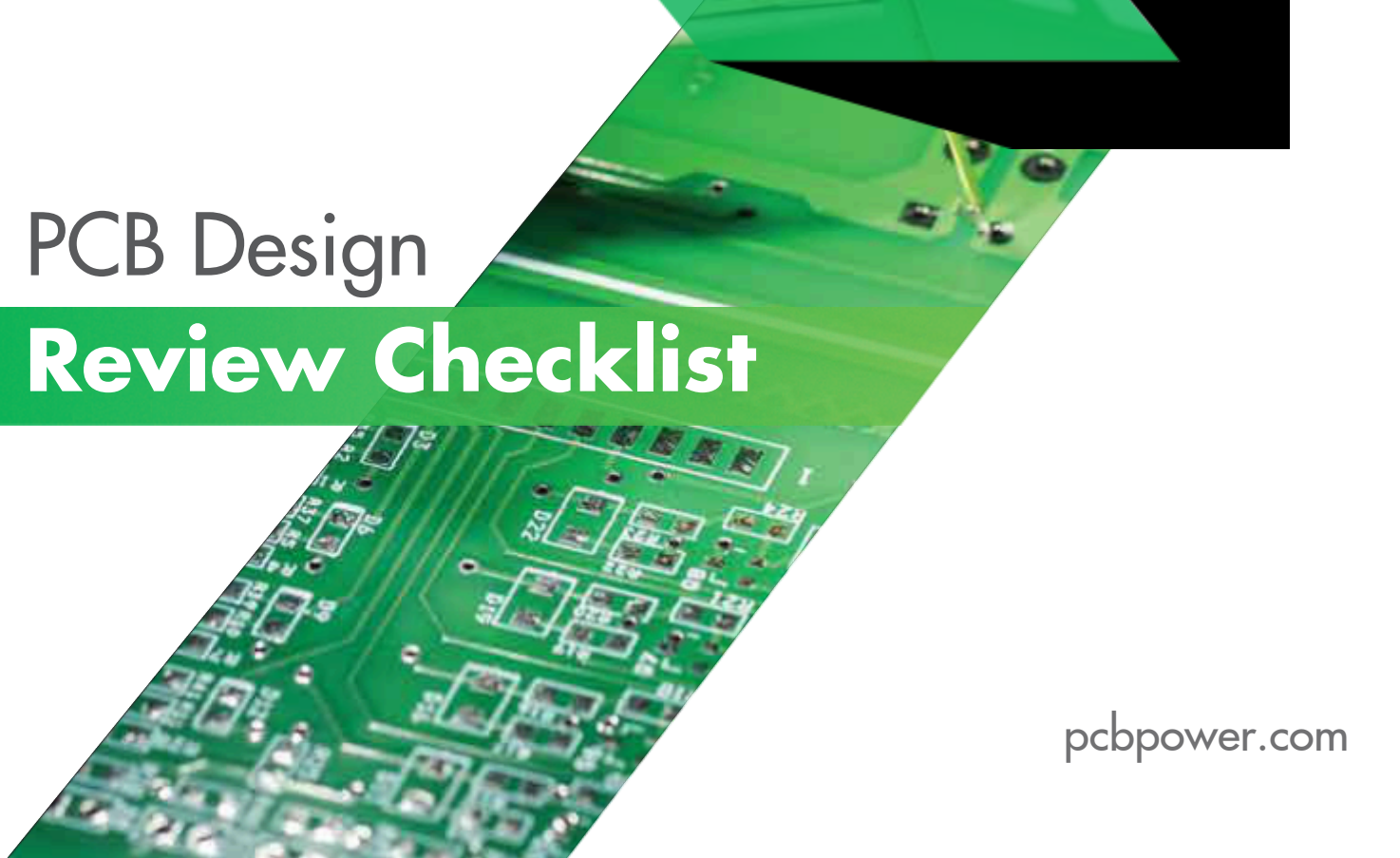
PCB Design **Review Checklist**



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PCB Design Review Checklist

Before Sending Your Design to Manufacturer

For: Designers | OEMs

How to Use This Checklist

Work through each section in order before generating your final data package. Tick each box when confirmed. Items marked ⚠ are critical — these are the most common causes of production holds, rejections, and respins at PCB Power.

Symbol	Meaning
□ Checkbox	Tick when item is verified. Write N/A if the item does not apply to your design.
⚠ Critical	High-priority item. PCB Power most commonly flags designs for these. Do not skip.
Specification column	PCB Power-specification or official design guideline.

Section 1 — Data Package & Gerber Output

Your Gerber data package is the primary manufacturing input. Errors here cause immediate production holds.

✓	Parameter	Why It Matters
	1A. File Format & Output Settings	
□	⚠ All files are in Gerber RS-274X format (not RS-274D)	*RS-274X required; RS-274D is obsolete*
□	⚠ NC Drill file is in Excellon 1 or 2 format with embedded tool list	*PCB Power specification*
□	⚠ Separate drill files for PTH and NPTH holes (or clearly marked different tools)	*PTH/NPTH must be distinguishable*
□	⚠ All data is at full scale — 1:1 ratio. No scaling applied.	*Scaled data causes wrong board size*
□	⚠ Same units (mm or inch) used consistently across all Gerber and Excellon files	*Prevents conversion/rounding errors*

✓	Parameter	Why It Matters
	1A. File Format & Output Settings	
☐	⚠️ Same offset (preferably zero) used for all Gerber layers and drill data	*Mismatched offsets cause layer misalignment*
☐	No zero-sized apertures (0.00 mm) in Gerber files; no zero-sized tools in Excellon	*Zero sizes have no physical meaning*
☐	File names are clear and short — layer function is identifiable from filename	*Long or unclear names cause confusion*
☐	A readme/fab notes file is included listing all files and special requirements	*Strongly recommended by PCB Power*
	1B. Gerber Layer Content Verification	
☐	⚠️ Package includes: all copper layers, solder mask, silkscreen, SMD paste, board outline/mechanical layer & drill layer	*All layers required*
☐	Carbon layer included (with board outline in layer) — if carbon contacts/printing specified	*Required if carbon finish ordered*
☐	Peel-off layer included (with board outline in layer) — if peel-off specified	*Required if peel-off ordered*
☐	Via Fill layer included (only via pads needing fill + board outline) — if via fill specified	*Required if via fill ordered*
☐	⚠️ Gerber output has been verified in a Gerber viewer before submission	*Critical self-check — do not skip*
☐	Board outline is included in each Gerber layer for alignment reference	*PCB Power specification*
☐	⚠️ Top-side text reads correctly (right-reading); bottom-side text is mirrored	*Prevents mirror/reversed production*
☐	Each Gerber layer labelled with top-viewed right-reading text to identify the layer	*Universal PCB industry convention*
☐	No original CAD files, PDFs, Word or Excel files included in the fabrication package	*Not required; causes confusion*

Section 2 — Drill Layer Review

Hole sizes, locations, and drill definitions must be reviewed carefully. Even small drill-related errors can affect reliability and manufacturability.

✓	Parameter	Why It Matters
	Drill Layer Checks	
☐	⚠️ No overlapping drill holes — each drill is a distinct, non-overlapping circle	*Overlapping holes break drill bits; cause barrel voids*
☐	⚠️ Slots defined using routing/milling outlines — NOT by chaining overlapping drills	*Overlapping drills for slots = manufacturing reject*
☐	All drill sizes within 0.05 mm (2 mil) of each other are combined into one tool size	*PCB Power specification*
☐	⚠️ PTH and NPTH holes use different tools, clearly marked in drill file	*Critical for process differentiation*
☐	NPTH holes on board contour are treated as part of the outline — correct outline drawn around them	*Prevents fabrication errors at board edge*
☐	PTH holes on board edge clearly mentioned in mechanical layer	*Edge PTH requires special handling*
☐	⚠️ Drill hole positions cross-checked against copper pads — no misalignment/offset	*Pad-to-hole offset violates annular ring*
☐	⚠️ NPTH Drill-to-copper (outer layer isolation) meets minimum supported value — refer to PCB Power technical capabilities page	Check *PCB Power specification*
☐	Inner layer Drill-to-copper isolation meets minimum supported value - refer to PCB Power technical capabilities page	*Check PCB Power specification*
☐	⚠️ Inner layer annular ring meets minimum supported value — no breakout risk	*Breakout = open connection/structural failure*
☐	⚠️ Outer layer annular ring meets minimum supported value — sufficient solderable land area	*Below minimum = poor solder joints, open circuits*

Section 3 — Copper Layer Review

Trace widths, clearances, and copper distribution directly affect board performance. Reviewing these layers helps ensure reliable manufacturing.

✓	Parameter	Why It Matters
	3A. Copper Design Rules	
☐	⚠️ Trace width and trace-to-trace spacing meet minimums for chosen copper weight	*≥ 0.10 mm (4 mil) for standard 1 oz Cu*
☐	⚠️ Outer layer isolation meets minimum supported value	*Below minimum = shorts risk*
☐	Inner layer isolation and track width account for final copper thickness (etch compensation)	*Over-etching or shorts if too narrow for specified finish Cu*
☐	⚠️ Copper pads use 'flash' definition — NOT drawn/painted with small vectors	*Drawn pads cause CAM issues and inconsistent output*
☐	⚠️ Copper planes/pours use polygon fills (contours) — NOT drawn fills or hatch painting	*Drawn planes cause interpretation and etching errors*
☐	Unconnected copper pads removed from NPTH holes	*Floating copper pads cause DRC false positives*
☐	⚠️ Copper pattern kept away from board edge	*Copper too close to edge is damaged during routing/scoring*
☐	If copper must extend to board edge (edge plating), this is clearly stated in mechanical layer	*Requires explicit note — special process*
☐	⚠️ No copper slivers — minimum 0.20 mm (8 mil) spacing between isolated pads in plane layers	*Slivers cause shorts/opens from resist lifting*
☐	No peelable mask errors or same-net spacing errors in copper layers	*Review with DRC before export*
☐	Full solid copper used in planes — not hatch — to avoid low-pressure lamination zones	*Hatch planes can cause micro-voids and delamination*
☐	Thermal relief correctly specified for all pads in copper planes — no thermal isolation	*Isolation = poor reflow; no relief = poor solderability*
☐	Thermal relief gap = 0.25 mm (10 mil); thermal segment width = 0.20 mm (8 mil)	*PCB Power specification*

✓	Parameter	Why It Matters
	3B. Multilayer Stack-up & Symmetry	
☐	⚠️ Layer sequence drawing (stack-up) included in mechanical layer with correct top-to-bottom order	*Required for multilayer*
☐	⚠️ Copper layers are symmetrical around the centre of the stack-up (balanced construction)	*Unbalanced stack causes bow and twist*
☐	Number and weight of copper layers is symmetrical around the centre	*Asymmetrical copper weight causes warpage*
☐	Plane layers placed at symmetrical locations in the stack-up	*Minimises warpage risk*
☐	Inner layers have venting or copper pattern to equalise pressure distribution	*Low-pressure zones cause micro-voids and delamination*
☐	Layer numbers indicated in each copper layer image (1 = top, increasing to bottom)	*Helps PCB Power verify correct layer order*
☐	Impedance-controlled traces are on the correct layers per the specified stack-up	*Wrong layer = impedance mismatch*

Section 4 — Solder Mask & Legend (Silkscreen)

Proper mask clearances and clear component identification are critical for assembly. A review here helps prevent avoidable production issues.

✓	Parameter	Why It Matters
	4A. Solder Mask	
☐	⚠️ Solder mask opening (growth) is ≥ 0.06 mm (2.36 mil) around each pad	*PCB Power specification*
☐	⚠️ Solder mask dam between adjacent pads is ≥ 0.08 mm (3.15 mil)	*Below 3.15 mil, dam can lift from PCB surface*
☐	Non-green solder mask: wider openings and bigger dams specified	*Non-green masks require more clearance*
☐	⚠️ Solder mask openings are ≥ 0.10 mm away from adjacent copper traces	*Prevents unintended trace exposure and shorts*
☐	⚠️ No solder mask over SMD pads — pads are fully open	*Covered pads prevent soldering*
☐	Solder mask side (top/bottom) unambiguously indicated in file naming or readme	*Prevents wrong-side masking*
	4B. Legend/Silkscreen	
☐	⚠️ All legend font heights are ≥ 1.00 mm (40 mil) — no smaller text used	*Below 1 mm becomes unreadable after printing*
☐	Legend line width is ≥ 0.10 mm (4 mil) — thinner lines removed	*PCB Power specification*
☐	⚠️ Legend does not overlap solder mask openings (pads) — clipped where needed	*Legend ink on pads interferes with soldering*
☐	Clearance between legend and copper image is ≥ 0.20 mm (8 mil)	*Prevents clipped or bleeding legend*
☐	Legend to PCB edge: ≥ 0.25 mm (routing), ≥ 0.45 mm (scoring)	*PCB Power specification*
☐	Legend to holes/cutouts clearance: ≥ 0.10 mm	
☐	Legend to exposed copper clearance: ≥ 0.10 mm	
☐	All reference designators visible, legible, and on the correct side of the board	*Aids assembly and inspection*
☐	⚠️ Pin 1/polarity markers present on all polarised components	*Missing polarity = wrong orientation risk*

Section 5 — Mechanical Layer & Board Outline

Board dimensions, cutouts, slots, and stack-up details must be clearly documented. Accurate mechanical data helps ensure a smooth manufacturing process.

✓	Parameter	Why It Matters
	Mechanical Layer Checks	
☐	⚠️ Mechanical layer contains exact board outline with dimensions in mm or inch	*Centre of contour line = actual board edge*
☐	⚠️ All internal milling, slots, and cutouts shown with exact positions and dimensions	*Required for accurate machining*
☐	⚠️ PTH and NPTH designation clearly indicated for all holes and slots	*Required for correct processing*
☐	⚠️ Layer sequence/stack-up drawing included in mechanical layer (top-to-bottom order with file names)	*Required for multilayer boards*
☐	Reference hole specified with X/Y distances from PCB outline — especially for NPTH without pads	*Required for accurate drill placement*
☐	Positional drill map using different symbols for each drill size is included	*Verifies drill file completeness*
☐	If boards delivered as assembly array, array mechanical drawing is included	*Required for panelised deliveries*
☐	Countersunk holes: mechanical drawing includes image showing actual diameter and angle values	*Required for accuracy*
☐	Any edge plating or special edge requirements clearly called out in mechanical layer	*Special process — must be explicit*
☐	GKO (Keep-Out) layer defined separately from mechanical outline where required	*GKO = design rule enforcement; mechanical = fab reference*

Section 6 — Special Process Layers

Carbon printing, peel-off masks, and via fill require additional layer verification. Reviewing these files ensures special requirements are correctly applied.

✓	Parameter	Why It Matters
	6A. Carbon Layer (skip if not applicable)	
☐	Carbon layer side (top, bottom, or both) stated in file name and mechanical layer	*PCB Power specification*
☐	Board outline included in carbon layer(s)	*Required for alignment*
☐	⚠ Minimum carbon line width: ≥ 0.30 mm (12 mil)	*PCB Power specification*
☐	⚠ Minimum carbon-to-carbon spacing: ≥ 0.254 mm (10 mil)	*PCB Power specification*
☐	Carbon pad is 0.15 mm (6 mil) larger than copper pad	*PCB Power specification*
☐	Mask pad is the same size as carbon pad	*PCB Power carbon specification*
	6B. Peel-off Mask (skip if not applicable)	
☐	Peel-off side stated in file name and mechanical layer (usually bottom side)	*PCB Power specification*
☐	Board outline included in peel-off layer	*Required for alignment*
☐	⚠ Minimum peel-off element width: ≥ 0.500 mm (20 mil)	*PCB Power specification*
☐	Maximum coverable hole endsize: ≤ 6.00 mm	*PCB Power specification*
☐	Minimum overlap on copper pattern: ≥ 0.254 mm (10 mil)	
☐	Minimum clearance to free copper: ≥ 0.254 mm (10 mil)	
☐	Minimum distance of peel-off from PCB outline: ≥ 0.500 mm (20 mil)	
☐	Merge peel-off areas into larger areas where practical (easier removal after soldering)	*Good practice as per PCB Power*

✓	Parameter	Why It Matters
	6C. Via Fill (skip if not applicable)	
□	Peel-off side stated in file name and mechanical layer (usually bottom side)	*PCB Power specification*
□	Board outline included in peel-off layer	*Required for alignment*
□	⚠️ Minimum peel-off element width: ≥ 0.500 mm (20 mil)	*PCB Power specification*
□	⚠️ All via holes requiring fill have endsize ≤ 0.25 mm (10 mil)	*Maximum size for guaranteed complete closure*
□	Via Fill side (top/bottom) stated in file name and mechanical layer	*PCB Power specification*

Section 7 — Schematic & Electrical Verification

A thorough schematic review helps eliminate shorts, opens, and connectivity errors. This step improves both reliability and production readiness.

✓	Parameter	Why It Matters
	Schematic & Electrical Checks	
☐	⚠️ ERC (Electrical Rules Check) run — zero errors remaining	*Open nets, floating pins, shorts must be resolved*
☐	Differential pairs correctly defined and matched in schematic	*Skew originates at schematic level*
☐	⚠️ No unintended net connections (shorts) or missing connections (opens)	*Most common schematic error*
☐	All component values, tolerances, and voltage ratings verified against design requirements	*Wrong rating = field failure*
☐	⚠️ Component polarity and pin-1 orientation confirmed in schematic and matched to footprint	*Reverse polarity = board damage/component destruction*
☐	High-speed interfaces (USB, Ethernet, DDR, etc.) follow reference design topology	*Impedance and topology must match interface specification*

Section 8 — Component Footprints & BOM

Each component must match its footprint, package, and manufacturer part number. Verification helps prevent costly assembly delays.

✓	Parameter	Why It Matters
	8A. Footprint Verification	
☐	⚠️ All footprints verified against component datasheet (pad size, pitch, pin count, pin-1 orientation)	*Wrong footprint = no solder/bridging*
☐	Courtyard/keepout defined for every component — no overlapping courtyards	*Clearance required for pick-and-place tooling*
☐	⚠️ Silkscreen reference designators do not overlap solder mask openings (pads)	*Required — legend on pads degrades soldering*
☐	⚠️ Pin-1/polarity indicator present on silkscreen for all polarised components	*Missing = assembly error risk*
☐	QFN/BGA/thermal pad footprints have correct exposed pad and thermal via array	*Thermal vias essential for power dissipation*
☐	IPC-7351 standard land pattern used, or datasheet-recommended pattern verified	*Non-standard pads cause yield issues*
☐	No components placed too close to board edge (clearance for routing and assembly)	*Risk of component damage during depanelisation*

✓	Parameter	Why It Matters
	8B. Bill of Materials (BOM)	
☐	⚠️ BOM contains: Ref-Des, Quantity, Description, Manufacturer Name, MPN	*Minimum required fields for assembly*
☐	BOM provided in CSV or XLS format	*PCB Power specification*
☐	⚠️ BOM contains: Ref-Des, Quantity, Description, Manufacturer Name, MPN	*Minimum required fields for assembly*
☐	⚠️ Every part has a valid, in-production MPN — no NRND or EOL parts	*Obsolete parts halt production*
☐	⚠️ Package/footprint in BOM matches the footprint in the layout (e.g. 0402 not 0603)	*Package mismatch = wrong component placed*
☐	Quantities in BOM match the reference designators in schematic and layout	*Mismatch = missing or excess parts*
☐	Alternate/approved parts listed for critical long-lead or scarce components	*Reduces procurement risk*
☐	BOM checked for duplicate reference designators	*Duplicates cause kitting errors*

Section 9 — DFM, Thermal & EMC

Manufacturing success depends on more than electrical functionality alone. DFM and thermal checks help ensure consistent build quality.

✓	Parameter	Why It Matters
	9A. Design for Manufacture (DFM)	
☐	⚠️ DRC (Design Rule Check) run against manufacturer's rule file — zero violations	*Catches spacing, annular ring, mask violations*
☐	⚠️ Fiducials provided: minimum 3 global on board edges; 2 local for fine-pitch ICs	*Required for pick-and-place alignment*
☐	No components or pads in V-score or depanelisation cut areas	*Components in cut zone get damaged*
☐	Paste stencil layer correctly defined — apertures do not exceed pad sizes	*Excess paste = solder bridging*
☐	Adequate spacing between SMD pads of adjacent components — no bridge risk	*Fine-pitch ICs most at risk*
☐	Double-sided SMT planned correctly — reflow sequence defined for both sides	*Requires separate planning if both sides have SMT*
☐	Board bow/twist expected within tolerance — balanced stack-up confirms this	*Excess warp causes SMT misplacement*
	9B. Thermal Management	
☐	⚠️ Power-dissipating components (regulators, MOSFETs, power ICs) have copper pours or thermal vias	*Heat must have an escape path*
☐	⚠️ QFN/DFN/BGA thermal pads have via array to inner plane layers	*Thermal vias essential for these packages*
☐	Thermal relief correctly set on through-hole pads in copper planes	*Balance solderability vs. heat conduction*
☐	Heatsink footprint/mounting holes included if heatsink required	*Mechanical fit must be verified*
	9C. Signal Integrity & EMC	
☐	High-speed traces routed on inner layers between ground and power planes	*Inner routing between planes reduces radiation*
☐	⚠️ Controlled impedance traces on correct stack-up layers per impedance calculation	*Specify stack-up to PCB Power for impedance control*

Section 10 — Testability (DFT)

Designing for test improves fault detection and troubleshooting. Accessible test points make validation faster and more reliable.

✓	Parameter	Why It Matters
	Design for Test Checks	
☐	⚠️ Test points present on all critical nets (power rails, clocks, key signals)	*Without test points, faults cannot be diagnosed*
☐	Test pad size ≥ 0.50 mm (20 mil) recommended; minimum 0.15 mm (6 mil)	*Larger pads allow reliable probe contact*
☐	Spacing between test pads ≥ 0.25 mm (10 mil)	*Prevents probe-to-probe shorts*
☐	Ground test points present at multiple locations — board corners preferred	*Reference points for test fixture/flying probe*
☐	Test pads not obstructed by components, heatsinks, or solder mask	*Covered test points are inaccessible*
☐	All nets accessible from one side of board where possible	*Single-side access simplifies test fixture/flying probe*
☐	Test point locations documented in assembly drawing or separate DFT document	*Aids test fixture design*

Section 11 — Final Pre-Submission Sign-Off

This final review helps ensure all manufacturing files are complete, accurate, and ready for production. A few minutes here can prevent days of delays.

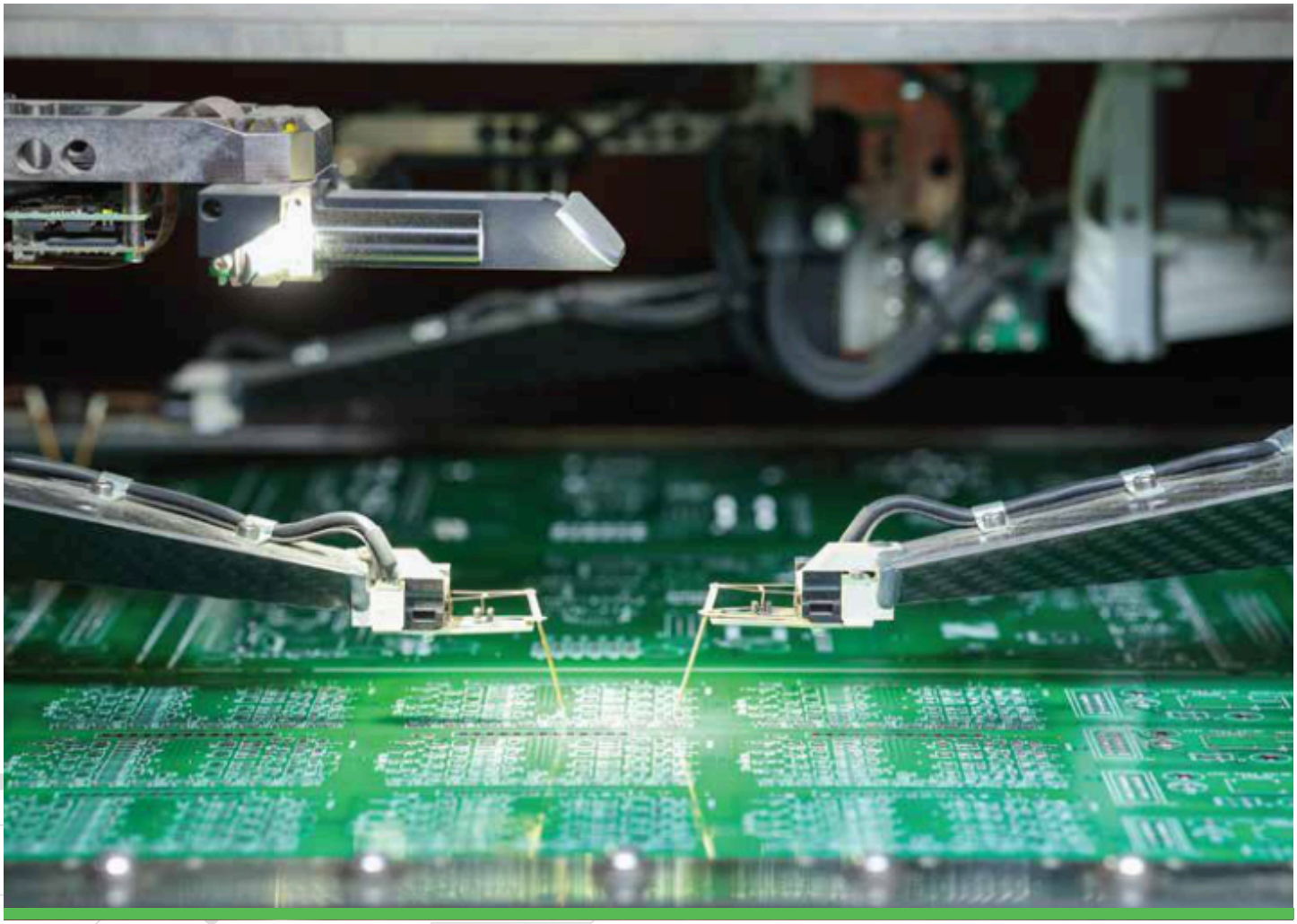
✓	Parameter	Why It Matters
	Final Check	
☐	⚠️ Gerber files verified in a Gerber viewer — all layers present and correct	*Do not skip this step*
☐	⚠️ Drill file verified — all holes visible, no zero-size tools, PTH/NPTH separated	*Critical data check*
☐	Readme/fab notes file included — file list, special requirements, FAQ answers	*Prevents unnecessary queries from PCB Power*
☐	Stack-up drawing included for multilayer and impedance-controlled boards	*Required for multilayer*
☐	⚠️ Mechanical drawing complete — outline, slots, holes, stack-up, layer names all present	*Incomplete mechanical layer is a common hold cause*
☐	⚠️ BOM verified — all MPNs active, packages correct, quantities match schematic, extra quantity added	*Wrong BOM = wrong parts assembled*
☐	Pick-and-place (CPL) file verified — X/Y, rotation, side, ref-des all present	*Required for assembly*
☐	⚠️ All files use consistent units, offset, and scale (1:1)	*Inconsistency causes layer misalignment*
☐	File naming is clear and matches readme description	*Prevents wrong-file processing*
☐	Tolerances confirmed or PCB Power defaults accepted: thickness ±10%, size ±0.25 mm, drill ±0.075 mm	*State explicitly in readme if different from default*
☐	⚠️ Special processes (carbon, peel-off, via fill, countersunk, edge plating) called out in readme/mechanical layer	*Missing callouts = process not applied*
☐	Panelisation requirement stated if boards to be delivered as array	*See pcbpower.com/panel-guidelines*
☐	Design revision/version number included in file name or readme	*Prevents old-revision mistakes*
☐	Customer reference/PO number included in submission notes	*Required for order tracking*

Reference: PCB Power DFM Parameters

Run through this immediately before zipping and submitting your data package to PCB Power.

Parameter	PCB Power Specification
Min. Trace Width (1 oz Cu)	≥ 0.09 mm (3.54 mil)
Min. Trace-to-Trace Spacing	≥ 0.09 mm (3.54 mil)
Min. Drill Hole Size (PTH)	≥ 0.20 mm (8 mil)
Drill Tolerance (PTH)	± 0.075 mm (± 3 mil)
PCB Thickness Tolerance	± 10%
PCB Size Tolerance	± 0.25 mm (± 10 mil)
Solder Mask Growth/Opening	≥ 0.06 mm (2.36 mil) around pad
Solder Mask Dam	≥ 0.08 mm (3.15 mil)
Mask-to-Copper Clearance	≥ 0.10 mm (4 mil)
Copper Sliver Spacing (plane)	≥ 0.20 mm (8 mil)
Legend Font Height	≥ 1.00 mm (40 mil)
Legend Line Width	≥ 0.10 mm (4 mil)
Legend-to-Copper Clearance	≥ 0.20 mm (8 mil)

Parameter	PCB Power Specification
Legend to PCB Edge (routing)	≥ 0.25 mm
Legend to PCB Edge (scoring)	≥ 0.45 mm
Legend to Holes/Cutouts	≥ 0.10 mm
Thermal Relief Gap	0.25 mm (10 mil)
Thermal Segment Width	0.20 mm (8 mil)
Carbon Line Width	≥ 0.30 mm (12 mil)
Carbon-to-Carbon Spacing	≥ 0.254 mm (10 mil)
Carbon Pad vs. Copper Pad	+ 0.15 mm (6 mil) larger
Peel-off Min. Element Width	≥ 0.500 mm (20 mil)
Peel-off Distance from Edge	≥ 0.500 mm (20 mil)
Via Fill Max. Hole Endsize	≤ 0.25 mm (10 mil)
Drill Step Increment	0.05 mm (2 mil)



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Over 30 Years of Excellence in PCB Manufacturing

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